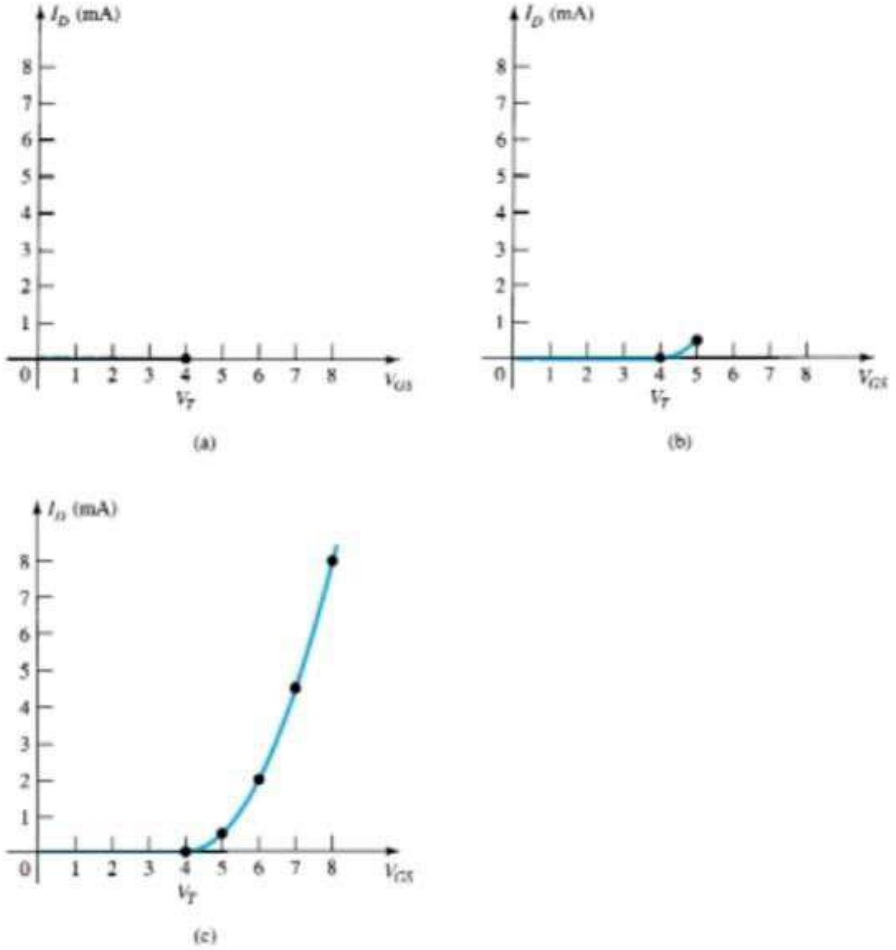

Figure 5.36 Plotting the transfer characteristics of an *n*-channel enhancement-type MOSFET with $k = 0.5 \times 10^{-3}$ A/V^2 and $V_T = 4$ V.

and a point on the plot is obtained as shown in Fig. 5.36b. Finally, additional levels of V_{GS} are chosen and the resulting levels of I_D obtained. In particular, at $V_{GS} = 6$, 7, and 8 V, the level of I_D is 2, 4.5, and 8 mA, respectively, as shown on the resulting plot of Fig. 5.36c.

p-Channel Enhancement-Type MOSFETs

The construction of a *p*-channel enhancement-type MOSFET is exactly the reverse of that appearing in Fig. 5.31, as shown in Fig. 5.37a. That is, there is now an *n*-type substrate and *p*-doped regions under the drain and source connections. The terminals remain as identified, but all the voltage polarities and the current directions are reversed. The drain characteristics will appear as shown in Fig. 5.37c, with increasing levels of current resulting from increasingly negative values of V_{GS}. The transfer characteristics will be the mirror image (about the I_D axis) of the transfer curve of Fig. 5.35, with I_D increasing with increasingly negative values of V_{GS} beyond V_T, as shown in Fig. 5.37b. Equations (5.11) through (5.14) are equally applicable to *p*-channel devices.

I_{DDS}/V_P

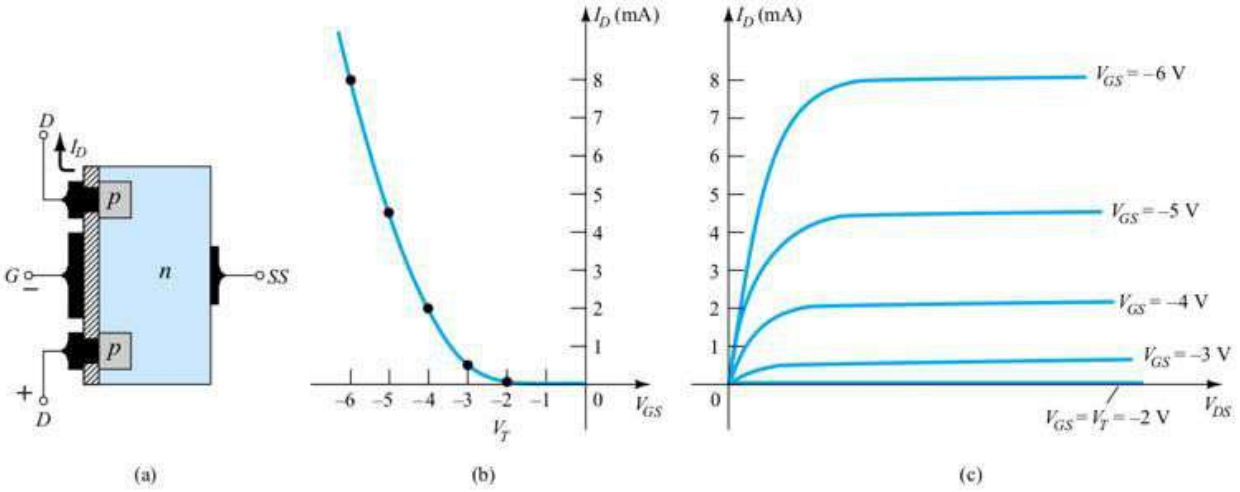

Figure 5.37 *p*-Channel enhancement-type MOSFET with $V_T = 2$ V and $k = 0.5 \times 10^{-3}$ A/V^2.

Symbols, Specification Sheets, and Case Construction

The graphic symbols for the *n*- and *p*-channel enhancement-type MOSFETs are provided as Fig. 5.38. Again note how the symbols try to reflect the actual construction of the device. The dashed line between drain and source was chosen to reflect the fact that a channel does not exist between the two under no-bias conditions. It is, in fact, the only difference between the symbols for the depletion-type and enhancement-type MOSFETs.

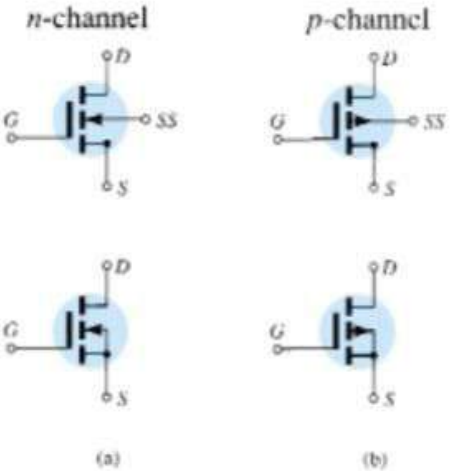

Figure 5.38 Symbols for (a) *n*-channel enhancement-type MOSFETs and (b) *p*-channel enhancement-type MOSFETs.

The specification sheet for a Motorola *n*-channel enhancement-type MOSFET is provided as Fig. 5.39. The case construction and terminal identification are provided next to the maximum ratings, which now include a maximum drain current of 30 mA dc. The specification sheet provides the level of I_{DSS} under "off" conditions, which is now simply 10 nA dc (at $V_{DS} = 10$ V and $V_{GS} = 0$ V) compared to the milliampere range for the JFET and depletion-type MOSFET. The threshold voltage is specified